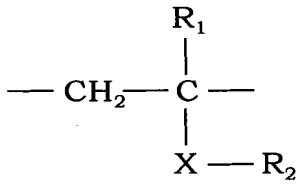
WHAT IS CLAIMED IS:

1. A via-filling material filled in a via hole previously when a trench wider than said via hole is formed by conducting plasma etching in via hole part in insulating film,

wherein said via-filling material comprises a polymer containing a repeat unit represented by the following formula (1):



(1)

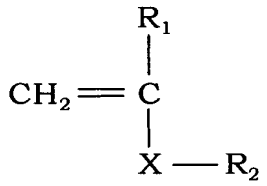
in which R_1 is a member selected from the group consisting of hydrogen atom, fluorine atom, chlorine atom, bromine atom and methyl group; R_2 is a member selected from the group consisting of hydrogen atom, C_{1-3} alkyl group and C_{1-4} alkyl group in which the hydrogen atom is substituted by at least one kind of atoms of fluorine, chlorine and bromine atom; and X is $-C(=O)O-$ or $-S(=O)_2O-$.

2. The via-filling material of Claim 1, wherein said polymer has a weight average molecular weight of 1,000 to 200,000.

3. A via-filling material filled in a via hole previously when a trench wider than said via hole is formed by conducting plasma etching in via hole part in insulating film,

wherein said via-filling material comprises a copolymer of a first monomer and a second monomer containing an unsaturated group

which brings about a copolymerization reaction with said first monomer and a functional group capable of crosslinking the copolymer, and wherein said first monomer being represented by the formula (2):



(2)

in which R_1 is a member selected from the group consisting of hydrogen atom, fluorine atom, chlorine atom, bromine atom and methyl group; R_2 is a member selected from the group consisting of hydrogen atom, C_{1-3} alkyl group and C_{1-4} alkyl group in which the hydrogen atom is substituted by at least one kind of atoms of fluorine, chlorine and bromine atom; and X is $-C(=O)O-$ or $-S(=O)_2O-$.

4. The via-filling material of Claim 3, wherein said functional group capable of crosslinking copolymer is an unsaturated group.

5. The via-filling material of Claim 3, wherein said functional group capable of crosslinking copolymer is an epoxy group.

6. A via-filling material comprising a mixture of the copolymer of Claim 4 and an unsaturated compound containing at least two unsaturated groups.

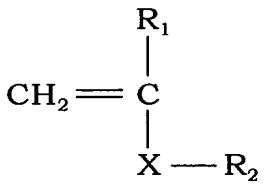
7. A via-filling material comprising a mixture of the copolymer of Claim 5 and an epoxy compound containing at least two

epoxy groups.

8. A via-filling material filled in a via hole previously when a trench wider than said via hole is formed by conducting plasma etching in a via hole part in insulating film,

wherein said via-filling material comprises a mixture obtained by mixing a compound selected from melamine compounds containing at least two methoxymethyl groups, urea compounds containing at least two methoxymethyl groups and epoxy compounds containing at least two epoxy groups to a copolymer of a first monomer and a second monomer, wherein said second monomer is an unsaturated compound containing a functional group selected from hydroxyl group, carboxyl group and dicarboxylic anhydride group, and

wherein said first monomer is represented by the formula (2):



(2)

in which R_1 is a member selected from the group consisting of hydrogen atom, fluorine atom, chlorine atom, bromine atom and methyl group; R_2 is a member selected from the group consisting of hydrogen atom, C_{1-3} alkyl group and C_{1-4} alkyl group in which the hydrogen atom is substituted by at least one kind of atoms of fluorine, chlorine and bromine atom; and X is $-C(=O)O-$ or $-S(=O)_2O-$.

9. A process for fabricating a semiconductor integrated

circuit, which comprises the steps of:

forming a stopper film on the surface of a lower insulating film on which a first conductor is formed and laminating an upper insulating film, interposing said stopper film;

forming a via hole leading from the surface of said upper insulating film to the surface of said stopper film at the position where said first conductor is located below;

applying the via-filling material of Claim 1 on the surface of said upper insulating film to fill said via hole with said via-filling material;

forming a resist pattern defining an opening part including said via hole on the applied film made of a via-filling body obtained by solidifying said via-filling material;

forming a trench of a depth which does not reach said stopper film in said upper insulating film by dry etching said upper insulating film and said via-filling body using said resist pattern as a mask;

removing said resist pattern, said applied film made of via-filling body and said via-filling body remaining in said via hole and etching said stopper film appeared on the bottom of said via hole, thereby exposing said first conductor; and

forming a second conductor in said trench and said via hole.

10. A process for fabricating a semiconductor integrated circuit, which comprises the steps of:

forming an insulating film on a substrate;

forming a via hole in said insulating film;

applying the via-filling material of Claim 1 on the surface of said insulating film to fill said via hole with said via-filling material;

forming a resist pattern defining an opening part including said via hole on the applied film made of a via-filling body obtained by solidifying said via-filling material;

forming a trench of a depth which does not reach said substrate in said insulating film by dry etching said insulating film and said via-filling body using said resist pattern as a mask;

removing said resist pattern, applied film made of via-filling body and via-filling body remaining in said via hole; and

forming a conductor in said trench and said via hole.

11. A process for fabricating a semiconductor integrated circuit, which comprises the steps of:

forming a stopper film on the surface of a lower insulating film on which a first conductor is formed and laminating an upper insulating film, interposing said stopper film;

forming a via hole leading from the surface of said upper insulating film to the surface of said stopper film at the position where said first conductor is located below;

applying the via-filling material of Claim 3 on the surface of said upper insulating film to fill said via hole with said via-filling material;

forming a resist pattern defining an opening part including said via hole on the applied film made of a via-filling body obtained by solidifying said via-filling material;

forming a trench of a depth which does not reach said stopper film in said upper insulating film by dry etching said upper insulating film and said via-filling body using said resist pattern as a mask;

removing said resist pattern, said applied film made of via-filling body

and said via-filling body remaining in said via hole and etching said stopper film appeared on the bottom of said via hole, thereby exposing said first conductor ; and

forming a second conductor in said trench and said via hole.

12. A process for fabricating a semiconductor integrated circuit, which comprises the steps of:

forming an insulating film on a substrate;

forming a via hole in said insulating film;

applying the via-filling material of Claim 3 on the surface of said insulating film to fill said via hole with the via-filling material;

forming a resist pattern defining an opening part including said via hole on the applied film made of a via-filling body obtained by solidifying said via-filling material;

forming a trench of a depth which does not reach said substrate in said insulating film by dry etching said insulating film and said via-filling body using said resist pattern as a mask;

removing said resist pattern, applied film made of via-filling body and via-filling body remaining in said via hole; and

forming a conductor in said trench and said via hole.

13. A process for fabricating a semiconductor integrated circuit, which comprises the steps of:

forming a stopper film on the surface of a lower insulating film on which a first conductor is formed and laminating an upper insulating film interposing said stopper film;

forming a via hole leading from the surface of said upper insulating film

to the surface of said stopper film at the position corresponding to said first conductor;

applying the via-filling material of Claim 8 on the surface of said upper insulating film to fill the via-filling material in said via hole;

forming a resist pattern defining an opening part including said via hole on the applied film made of a via-filling body obtained by solidifying said via-filling material;

forming a trench of a depth which does not reach said stopper film in said upper insulating film by dry etching said upper insulating film and said via-filling body using said resist pattern as a mask;

removing said resist pattern, said applied film made of via-filling body and said via-filling body remaining in said via hole and etching said stopper film appeared on the bottom of said via hole, thereby exposing said first conductor; and

forming a second conductor in said trench and said via hole.

14. A process for fabricating a semiconductor integrated circuit, which comprises the steps of:

forming an insulating film on a substrate;

forming a via hole in said insulating film;

applying the via-filling material of Claim 8 on the surface of said insulating film to fill the via-filling material in said via hole;

forming a resist pattern defining an opening part including said via hole on the applied film made of a via-filling body obtained by solidifying said via-filling material;

forming a trench of a depth which does not reach said substrate in said insulating film by dry etching said insulating film and said via-filling

body using said resist pattern as a mask;

removing said resist pattern, applied film made of via-filling body and via-filling body remaining in said via hole; and

forming a conductor in said trench and said via hole.